

REMARKS

Prior to the present amendment and response, claims 1-14 were pending in the present application. By this amendment, Applicant has amended claims 1 and 8, and has canceled claims 3 and 10. Thus, claims 1-2, 4-9, and 11-14 remain in the present application. Reconsideration and allowance of pending claims 1-2, 4-9, and 11-14 in light of the above amendments and the following remarks are respectfully requested.

A. Rejections of Claims 1-6 and 8-13 Under 35 USC § 102(b) and Claims 7 and 14 Under 35 USC § 103(a)

The Examiner has rejected claims 1-6 and 8-13 Under 35 USC § 102(b) as being anticipated by U.S. Patent 6,147,379 to Hori (hereinafter "Hori"). The Examiner has separately rejected claims 7 and 14 under 35 USC § 103(a) as being unpatentable over Hori in view of U.S. Patent 6,721,205 to Kobayashi (hereinafter "Kobayashi"). For the following reasons, Applicant respectfully submits that the amended claims are patentably distinguishable over the cited art.

The present invention, as defined by the amended claims, defines a floating gate memory cell where a "Vss connection region" under a recess and under a source of the floating gate memory cell is heavily doped so as to dramatically reduce the "Vss resistance," i.e. the resistance present in ground interconnection feeding common source areas in a memory array. In the absence of the present invention, the Vss resistance

results in significant voltage drop and power consumption and drastically impairs the performance of the memory array.

Moreover, the invention's floating gate memory cell with a Vss connection region under a recess and under a source of the floating gate memory cell, where the Vss connection regions is heavily doped, also prevents an increase in the pernicious DIBL (drain induced barrier lowering) problem. In the absence of the present invention, an increase in the source region doping level to achieve a lower Vss resistance would automatically worsen the DIBL problem.

Applicant respectfully submits that the structure of Hori does not teach, disclose, or even suggest the advantageous structure of the present invention as claimed by the amended claims. Moreover, Hori certainly is not directed to, nor does it achieve the advantages of the present invention embodied in the amended claims. Hori is directed to increasing electron injection efficiency in performing write operations, improving erase operations when taking out electrons from the floating gate into the drain region, suppressing the injection of holes into the oxide film when data is erased, increasing read current, and suppressing the degradation of the read disturb margin. See, for example, column 7, lines 5 through 20 of Hori. Among its long list of goals and achievements, Hori does not mention a word about lowering ground resistance (or Vss resistance) in the memory array. Nor does Hori mention a word about the harmful DIBL effects, to which the present invention is directed.

In describing its Figure 1A (the Figure to which the Examiner has referred), Hori acknowledges that: “The nonvolatile semiconductor memory device shown in FIGS. 1A and 1B is *principally characterized* in (1) that the drain region 8 has a triple structure consisting of the high-concentration drain region 8a, the low-concentration drain region 8b and the extremely-low-concentration drain region 8c, (2) that the low-concentration drain region 8b is formed so as to cover the corner portion at the bottom of the step, (3) that the extremely-low-concentration drain region 8c is formed in the step side region 13 and (4) that the steps have been formed in accordance with an epitaxial growth.” Column 11, lines 5-14 of Hori (emphasis added).

Thus, in achieving its write/erase objectives discussed above, Hori focuses on the configuration of the drain region used for writing and erasing data (and not the source region used for providing a ground connection). In this regard, Hori states:

“Since this device has such a drain structure, when a voltage of about 5 V is applied to the drain region 8 in writing data, the extremely-low-concentration drain region 8c is depleted. In this case, since the low-concentration drain region 8b has a higher impurity concentration than that of the extremely-low-concentration drain region 8c, only a part of the low-concentration drain region 8b (i.e., a part adjacent to the extremely-low-concentration drain region 8c) is depleted. *As a result, a high electric field is formed* in the corner portion between the second surface region 12 and the step side region 13” Column 11, lines 15-25 of Hori (emphasis added). Thus, Hori in fact teaches away from

reducing the DIBL problem which requires a lowering of, and not increasing, the electric field adjacent to the drain.

With reference to Figure 1A, Hori does state that: "The source region 7 formed in the first surface region 11 and the third surface region 14 includes a high-concentration impurity layer 7a and a low-concentration impurity layer 7b having an impurity concentration lower than that of the high-concentration impurity layer 7a." Hori, column 9, line 64 through column 10, line 1. However, as clearly shown in Figure 1B (which is the top view of Figure 1A), the region covered by layer 7a includes the "relatively high level (a first surface region 11)" (See Hori, column 8, lines 50-51). In other words, a substantial portion of Hori's "Vss connection region" is at the same elevation level as Hori's "source 7b." Therefore, in Hori, the Vss connection region is not under the source region, as required by the present invention. Thus, not only Hori fails to address the goals of the present invention, but also the invention's structure, as claimed by amended independent claims 1 and 8, is patentably distinguishable over Hori's disclosed structure.

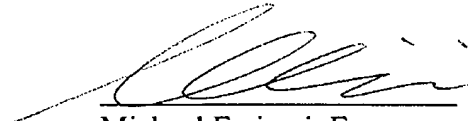
B. Conclusion

For all the foregoing reasons, the present invention as defined by the amended independent claims, is patentably distinguishable over Hori. Thus, the dependent claims are also patentably distinguishable over Hori, either singly or in combination with Kobayashi. As such, Applicant submits that all remaining claims 1-2, 4-9, and 11-14 are

Attorney Docket No.: 0180192

now in condition for allowance and an early Notice of Allowance directed to claims 1-2,
4-9, and 11-14 is respectfully requested.

Attorney Docket No.: 0180192

Respectfully Submitted,
FARJAMI & FARJAMI LLPDated: 10/6/05
Michael Farjami, Esq.
Reg. No. 38,135FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number 571-273-8300 on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 10/6/05Christina L Carter
Name of Person Performing Facsimile TransmissionChristina L Carter 10/6/05
Signature DateCERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: _____

Name of Person Mailing Paper and/or Fee _____

Signature _____ Date _____